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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/577,012	05/24/2000	Mohan Kalkunte	P108339-9017	5213

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EXAMINER

WAHBA, ANDREW W

ART UNIT PAPER NUMBER

2661

DATE MAILED: 08/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/577,012

Applicant(s)

KALKUNTE ET AL.

Examiner

Andrew W Wahba

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05/24/2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-29 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☒ Claim(s) 13-15 is/are objected to.
- 8) ☒ Claim(s) 16-29 are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 May 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 05/25/04 have been fully considered but they are not persuasive.

With regard to claim 1, the applicant argues that Onishi does not disclose a flow control unit. Onishi et al discloses a router manager 2 (flow control unit) that distributes a routing table to routing accelerators 3 that perform route selection (distribute a data load) on the basis of the routing table (column 7, line 9-15).

The applicant also argues that the claimed trunk group and the bus disclosed by Onishi are not equivalent. While the applicant describes the difference between the disclosed the claimed trunk group and the bus disclosed by Onishi on page 4, these differences are not claimed.

Also with regard to claim 1, the applicant argues that Haddock fails to disclose a flow control unit. Haddock discloses a buffer manager (flow control unit) that controls and coordinates access (distribute a load) to and from the packet RAM 125 (column 4, lines 30-34).

The applicant also argues that the claimed trunk group and the switch matrix disclosed by Haddock are not equivalent. While the applicant describes the difference between the disclosed the claimed trunk group and the switch matrix disclosed by Haddock on pages 5 and 6, these differences are not claimed.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this

Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 1-3 and 8-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Onishi et al (5,434,863). With regard to claim 1, Onishi et al discloses a communication port 53 of Ethernet as LAN of 100 Mbps (first data port interface) (column 7, lines 31-33). Onishi et al further discloses a communication port 54 of token ring LAN as LAN of 4-16 Mbps (second data port interface) (column 7, lines 33-34). Onishi et al further discloses a router manager 2 (flow control unit) that distributes a routing table to routing accelerators 3 that perform route selection (distribute a data load) on the basis of the routing table (column 7, line 9-15). Onishi et al further discloses a bus 4 (trunk group) (column 7, lines 17-18).

With regard to claim 2, Onishi et al further discloses a router manager 2 that acts as a main processor (CPU) (column 7, line 4-6). The routing manager 2 is connected (CPU interface) to the router bus 1 (communication channel) (column 7, lines 3-4).

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With regard to claim 3, Onishi et al discloses a communication port 53 of Ethernet as LAN of 100 Mbps (Ethernet data port interface) (column 7, lines 31-33).

With regard to claims 8 and 9, Onishi et al further discloses that the router manager 2 is connected (CPU interface) to the router bus 1 (communication channel) (column 7, lines 3-4). Onishi et al further discloses that the router manager has the function of managing the whole system and the function of producing/distributing a routing table (program the operation) (column 7, lines 4-6).

With regard to claims 10 and 11, Onishi et al discloses a communication port 53 of Ethernet as LAN of 100 Mbps (maximum of 100 Mbps) (column 7, lines 31-33). A rate of 10 Mbps is included in the range 0-100 Mbps.

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who

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has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5. Claim 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Haddock et al (6,104,700). Haddock et al discloses an octal fast Ethernet interface (first data port interface) (column 4, lines 23-25 and Figure 1A). With regard to claim 1, Haddock et al further discloses a gigabit Ethernet interface 105 (second data port interface) (column 4, lines 19-23 and Figure 1A). Haddock et al further discloses a filtering/forwarding engine 115. Haddock et al further discloses that the filtering /forwarding engine includes a switch matrix (trunk group) (column 4, line 27). The switch matrix connects each channel to a central memory, packet RAM 125, and a buffer manager (flow control unit) that controls and coordinates access (distribute a load) to and from the packet RAM 125 (column 4, lines 30-34).

With regard to claim 2, Haddock et al further discloses that a CPU 130 (applicant's CPU) is coupled (applicant's CPU interface) to the forwarding/filtering engine 115 that includes a switch matrix (communication channel) (column 4, lines 15-18 and column 4, line 27).

With regard to claim 3, Haddock et al further discloses an octal fast Ethernet interface 110 (Ethernet data port interface) (column 4, lines 23-25 and Figure 1A).

With regard to claim 4, Haddock et al further discloses a gigabit Ethernet interface 105 (gigabit Ethernet data port interface) (column 4, lines 23-25 and Figure 1A).

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With regard to claim 6, Haddock et al further discloses a forwarding database 120 that stores information useful for making layer 2 decisions (layer two switching) (column 4, lines 35-37).

With regard to claim 7, Haddock et al further discloses a forwarding database 120 that stores information useful for making layer 3 decisions (applicant's layer three switching) (column 4, lines 35-37).

With regard to claims 8 and 9, Haddock et al further discloses that a CPU 130 (CPU) is coupled (CPU interface) to the forwarding/filtering engine 115 that includes a switch matrix (communication channel) (column 4, lines 15-18 and column 4, line 27). Haddock et al further discloses a packet RAM 125 for adapting (program the operation) between incoming and outgoing bandwidth differences (column 4, lines 48-50).

With regard to claims 10 and 11, Haddock et al further discloses an octal fast Ethernet interface 110 (column 4, lines 19-23 and Figure 1A). Data rates of 10/100 Mbps are supported.

With regard to claim 12, Haddock et al further discloses a gigabit Ethernet interface 105 (column 4, lines 19-23 and Figure 1A). A gigabit Ethernet interface supports a data rate of 1000 Mbps.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Onishi et al. With respect to claim 5, Onishi et al does not teach the placement of the first data port interface, second data port interface, CPU interface and communication channel on a single integrated chip. A person of ordinary skill in the art would have been motivated to integrate these components onto a single chip by the constant desire for smaller integrated electronic devices. At the time the invention was made, therefore, have been obvious to one of ordinary skill in the art to integrate these components onto a single chip as specified in claim 5.

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Haddock et al. With respect to claim 5, Haddock et al does not explicitly teach the placement of the first data port interface, second data port interface, CPU interface and communication channel on a single integrated chip. A person of ordinary skill in the art would have been motivated to integrate these components onto a single chip by the constant desire for smaller integrated electronic devices. At the time the invention was made, therefore, have been obvious to one of ordinary skill in the art to integrate these components onto a single chip as specified in claim 5.

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Allowable Subject Matter

9. Claims 13-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

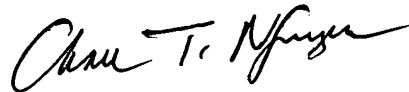
11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew W Wahba whose telephone number is (703) 305-4684. The examiner can normally be reached on M-F 8:30-5:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Douglas W Olms can be reached on (703) 305-4703. The fax phone

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number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Andrew Wahba *AW*
July 27, 2004



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